Complete Listing of Claims

This listing of claims will replace all prior versions and listings of claims in the application. Claim 17 is cancelled. No claims are amended or added in this response.

1. (Cancelled)

2. (Previously amended) The semiconductor device of claim 57 wherein the silicide is selected from the group consisting of cobalt silicide, platinum silicide, nickel silicide, chromium silicide, palladium silicide, tantalum silicide, and niobium silicide.

3. (Previously amended) The semiconductor device of claim 2 wherein the grown dielectric antifuse layer comprises silicon oxide.

4. (Previously amended) The semiconductor device of claim 2 wherein the grown dielectric antifuse layer comprises nitrogen.

5. (Previously amended) The semiconductor device of claim 4 wherein the grown dielectric antifuse layer comprises silicon nitride or silicon oxynitride.

6. (Previously amended) The semiconductor device of claim 2 wherein the conductive layer or semiconductor layer on and in contact with the grown dielectric antifuse layer is a conductive layer.

7. (Previously amended) The semiconductor device of claim 6 wherein the grown dielectric antifuse layer is less than about 50 angstroms thick.

8. (Original) The semiconductor device of claim 6 further comprising a first silicon layer, the silicide layer on and in contact with the first silicon layer.

9. (Previously amended) The semiconductor device of claim 2 wherein the conductor or semiconductor layer on and in contact with the grown dielectric antifuse layer is a lightly doped or intrinsic semiconductor layer.

10. (Previously amended) The semiconductor device of claim 9 wherein the lightly doped or intrinsic semiconductor layer forms a portion of a Schottky diode.

11. (Previously amended) The semiconductor device of claim 10 wherein the lightly doped or intrinsic semiconductor layer forms a portion of a Schottky diode after breakdown of the grown dielectric antifuse layer.

12. (Original) The semiconductor device of claim 11 wherein the Schottky diode is a portion of a memory cell.

13. (Original) The semiconductor device of claim 12 wherein the memory cell is a portion of a memory array.

14. (Original) The semiconductor device of claim 13 wherein the memory array is a monolithic three dimensional memory array.

15. (Original) The semiconductor device of claim 6 wherein the conductive layer comprises a metal.

16. (Original) The semiconductor device of claim 15 wherein the conductive layer forms a portion of a Schottky diode.

17. (Cancelled)

18. (Original) The semiconductor device of claim 17 wherein the Schottky diode is a portion of a memory cell.

19. (Original) The semiconductor device of claim 18 wherein the memory cell is a portion of a memory array.

20. (Original) The semiconductor device of claim 19 wherein the memory array is a monolithic three dimensional memory array.

21.-26. (Cancelled)

27. (Original) The semiconductor device of claim 6 wherein the conductive layer comprises titanium nitride.

28. (Original) The semiconductor device of claim 27 wherein the conductive layer forms a portion of a Schottky diode.

29. (Cancelled)

30. (Previously amended) The semiconductor device of claim 28 wherein the Schottky diode is a portion of a memory cell.

31. (Original) The semiconductor device of claim 30 wherein the memory cell is a portion of a memory array.

32. (Original) The semiconductor device of claim 31 wherein the memory array is a monolithic three dimensional memory array.

33. (Original) The semiconductor device of claim 27 wherein, for any portion of the conductive layer more than about 20 angstroms thick, the density of the titanium nitride is less than about 4.0 grams per cubic cm.

34. (Original) The semiconductor device of claim 27 wherein, for any portion of the film more than about 20 angstroms thick, the resistivity of the titanium nitride is greater than about 300 microOhm-cms.

35. (Previously amended) The semiconductor device of claim 2 wherein the grown dielectric antifuse layer was grown by oxidizing or nitriding the silicide.

36. (Previously amended) The semiconductor device of claim 2 wherein the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between a Schottky diode and a conductor.

37. (Original) The semiconductor device of claim 36 wherein the Schottky diode is a portion of a memory cell.

38. (Original) The semiconductor device of claim 37 wherein the memory cell is a portion of a memory array.

39. (Original) The semiconductor device of claim 38 wherein the memory array is a monolithic three dimensional memory array.

40. (Original) The semiconductor device of claim 36 wherein the silicide is a portion of the Schottky diode.

41. (Previously amended) The semiconductor device of claim 2 wherein the electrical connection between the silicide layer and the conductive layer or semiconductor layer is an electrical connection between portions of a Schottky diode.

42. (Original) The semiconductor device of claim 41 wherein the Schottky diode is a portion of a memory cell.

43. (Original) The semiconductor device of claim 42 wherein the memory cell is a portion of a memory array.

44. (Original) The semiconductor device of claim 43 wherein the memory array is a monolithic three dimensional memory array.

45. (Withdrawn) A monolithic three dimensional memory array comprising:

a first rail, wherein the first rail comprises a first silicon layer, a first silicide layer, and a first dielectric layer, the first silicide layer on and in contact with the first silicon layer and the first dielectric layer on and in contact with the first silicide layer; and

a second rail, wherein the second rail comprises a second silicon layer, wherein the second silicon layer is on and in contact with the first dielectric layer.

46. (Withdrawn) The array of claim 45 wherein the first silicide layer comprises a silicide selected from the group consisting of cobalt silicide, platinum silicide, nickel silicide, chromium silicide, palladium silicide, tantalum silicide, and niobium silicide.

47. (Withdrawn) The array of claim 46 wherein the first dielectric layer is grown.

48. (Withdrawn) The array of claim 47 wherein the first silicide layer and the second silicon layer operate as a Schottky diode after dielectric rupture of the first dielectric layer.

49. (Withdrawn) A monolithic three dimensional memory array comprising:

a first memory level formed at a first height above a substrate, wherein the first memory level comprises a silicide layer and a dielectric layer grown on the silicide layer; and

a second memory level formed at a second height above a substrate, the second height different from the first height.

50. (Withdrawn) The array of claim 49 wherein the silicide is selected from the group consisting of cobalt silicide, platinum silicide, nickel silicide, chromium silicide, palladium silicide, tantalum silicide, and niobium silicide.

51. (Withdrawn) The array of claim 50 wherein the dielectric layer comprises silicon oxide.

52. (Withdrawn) The array of claim 50 wherein the dielectric layer comprises nitrogen.

53. (Withdrawn) The array of claim 52 wherein the dielectric layer comprises silicon nitride.

54. (Withdrawn) The array of claim 52 wherein the dielectric layer comprises silicon oxynitride.

55. (Withdrawn) The array of claim 50 further comprising junction diodes.

56. (Withdrawn) The array of claim 50 further comprising a) Schottky diodes or b) Schottky diode portions, wherein the diode portions operate as a Schottky diode after dielectric rupture of an antifuse.

57. (New) A semiconductor device comprising:

a silicide layer;

a grown dielectric antifuse layer on and in contact with the silicide layer; and

a conductive layer or semiconductor layer on and in contact with the grown dielectric antifuse layer,

wherein the silicide layer and the grown dielectric antifuse layer are portions of the semiconductor device, and wherein the grown dielectric antifuse layer has suffered dielectric breakdown, such that an electrical connection exists between the silicide layer and the conductive layer or semiconductor layer.